diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond, wherein the diffusion barrier layer is constructed and arranged to mitigate inter-metallic compounds forming as a reaction to the metal layer connecting to the wire bond.

11. (*Amended*) A semiconductor chip having circuitry, the semiconductor chip comprising:

an aluminum bond pad over the circuitry and insulated on at least two sides by passivation material;

a diffusion barrier layer, including TiN, over the aluminum bond pad, at least two entire sides of the diffusion layer being insulated by the passivation material; and

a metal layer over the circuitry, the metal bond pad, the diffusion barrier layer, and at least partially over, and in contact with, a portion of the passivation material not over the diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond and the diffusion barrier layer being constructed and arranged to mitigate inter-metallic aluminum-based compounds forming as a reaction to the metal layer connecting to the wire bond.

12. (*Amended*) The semiconductor chip of claim 11, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron, the metal layer has a thickness that is at least 3 microns.

14. (*Amended*) A semiconductor chip having circuitry, the semiconductor chip comprising:

an aluminum bond pad over the circuitry and insulated on at least two sides by means for electrically insulating the aluminum bond pad;

barrier means, including TiN, over the aluminum bond pad, at least two entire sides of the diffusion layer being insulated by the passivation material; and

a metal layer over the circuitry, the metal bond pad, the barrier means, and at least partially over, and in contact with, a portion of the means for electrically insulating the aluminum bond pad not over the barrier means, the metal layer being configured and arranged for connecting to a wire bond and the barrier means for mitigating inter-metallic aluminum-based compounds forming as a reaction to the metal layer connecting to the wire bond.

15. (*New*) A semiconductor chip having circuitry, the semiconductor chip comprising:

a metal bond pad over a portion of the circuitry;

a diffusion barrier layer over the metal bond pad; and

a metal layer over the diffusion barrier layer, the metal layer being configured and arranged for connecting to a wire bond, and the metal bond pad, the diffusion barrier layer and the metal layer all being insulated on at least two sides by passivation material,

wherein the diffusion layer is constructed and arranged to mitigate inter-metallic compounds forming as a reaction to the metal layer connecting to the wire bond, and the passivation material is constructed and arranged to be at least partially over the metal bond pad, the passivation material and the diffusion layer.

16. (*New*) The semiconductor chip of claim 15, wherein the diffusion barrier layer includes TiN.

17. (*New*) The semiconductor chip of claim 16, wherein the diffusion barrier layer is further constructed and arranged to mitigate inter-metallic Al/Au compounds forming as a reaction to the metal layer connecting to the wire bond.

18. (*New*) The semiconductor chip of claim 15, wherein the diffusion barrier layer has a thickness that is at least 0.5 micron.

19. (*New*) The semiconductor chip of claim 18, wherein the metal layer has a thickness that is at least 3 microns.

20. (*New*) The semiconductor chip of claim 1, wherein the semiconductor chip is configured and arranged as a flip chip.

Remarks

The Office Action mailed June 5, 2002 indicated that claims 1, 2, 5-8, 10-11 and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Camilletti et al.* (U.S. Patent No. 5,693,565); and claims 3-4, 9 and 12-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Camilletti et al.* in view of *Shangguan et al.* (U.S. Patent No. 6,082,610). In